Ahsanullah University of Science and Technology

Department of Electrical and Electronic Engineering

LABORATORY MANUAL

FOR

ELECTRICAL AND ELECTRONIC SESSIONAL COURSES

Student Name :

Student ID :

Course no : EEE - 2104

Course Title : Electronic Circuits - I Lab

For the students of

Department of Electrical and Electronic Engineering

2nd Year, 1st Semester

Price : Tk. 14.00

Experiment No: 1

Name of the Experiment : I-V Characteristics of diode.

Objective :

Study the I-V characteristic of diode.

Theory :

A diode is a bi-polar device that behaves as the short circuit when it is in forward bias and as an open circuit when it is in reverse bias condition.

Figure 1.1 : Schematic Diagram of Diode.

Figure 1.2 : P - N Junction Diode .

There are two types of biasing condition for a diode :

1. When the diode is connected across a voltage source with positive polarity of source connected to p side of diode and negative polarity to n side, then the diode is in forward bias condition.
2. When the diode is connected across a voltage source with positive polarity of source connected to n side of diode and negative polarity to p side, then the diode is in reverse bias condition.

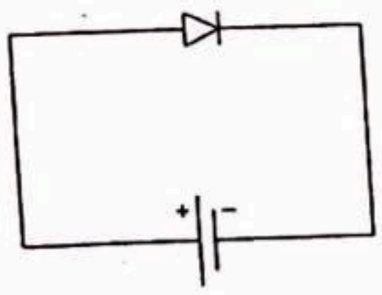


Figure 1.3 : Forward Bias connection.

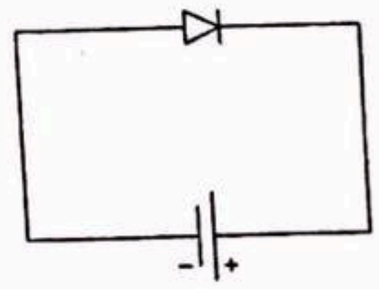


Figure 1.4 : Reverse Bias connection.

If the input voltage is varied and the current through the diode corresponds to each voltage are taken then the plot of diode current (I_d) vs diode voltage (V_D) will be follows :

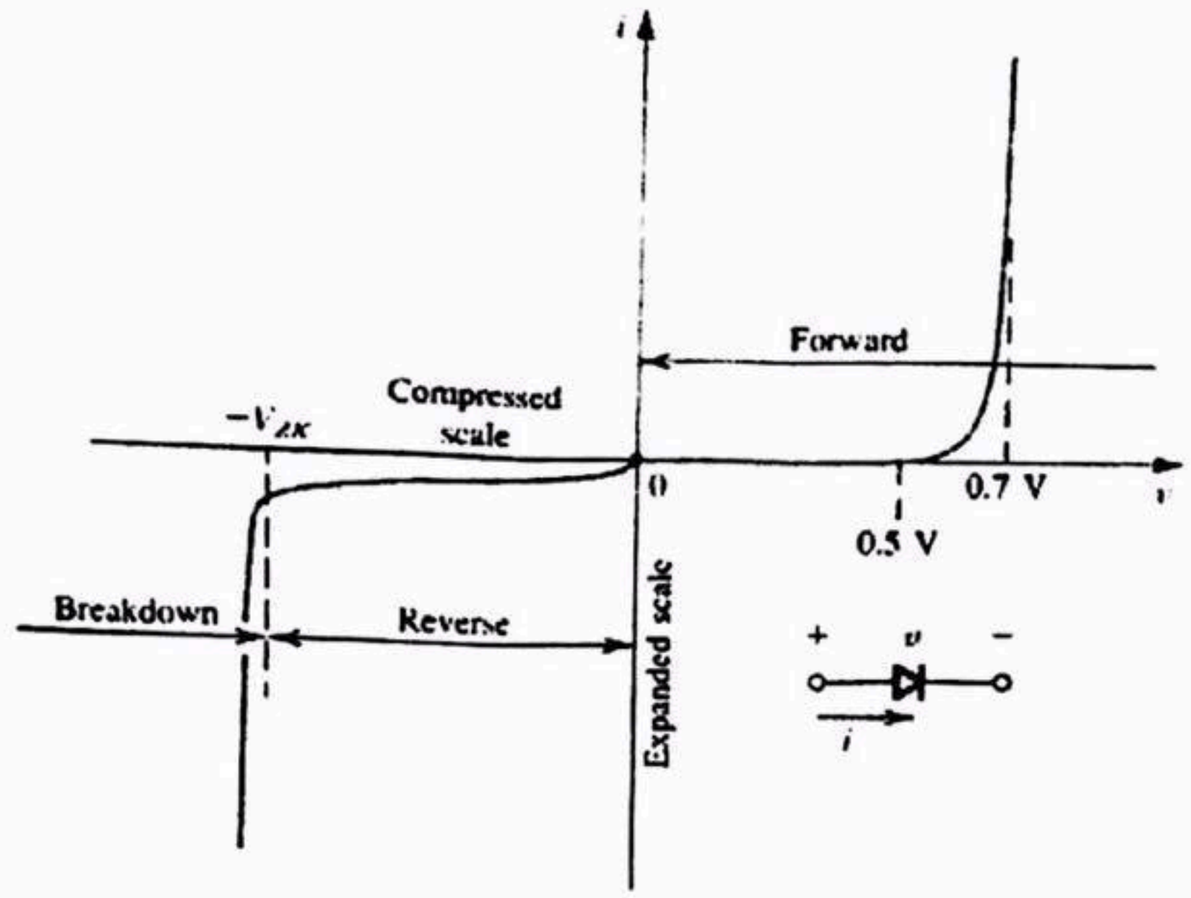


Figure 1.5 : I - V Characteristics of Diode.

At the reverse bias condition the amount of current flows through the diode is very small (at microampere range). But if the voltage continuously increases in reverse direction, at a certain value the diode will break down and huge amount of current will flow in reverse direction. This is called breakdown of diode. In laboratory the breakdown will not tested because it will damages the diode permanently.

From the characteristics curve it can be seen that, a particular forward bias voltage (V_T) is required to reach the region of upward swing. This voltage, V_T is called the cut-in voltage or threshold voltage of diode. For Si diode the typical value of threshold voltage is 0.7 volt and for Ge diode is 0.3 volt.

Equipments And Components :

Serial no.	Component Details	Specification	Quantity
1.	p-n junction diode	1N4007	1 piece
2.	Resistor	1 KΩ	1 piece
3.	DC power supply		1 unit
4.	Signal generator		1 unit
5.	Trainer Board		1 unit
6.	Oscilloscope		1 unit
7.	Digital Multimeter		1 unit
8.	Chords and wire		as required

Experimental Setup :

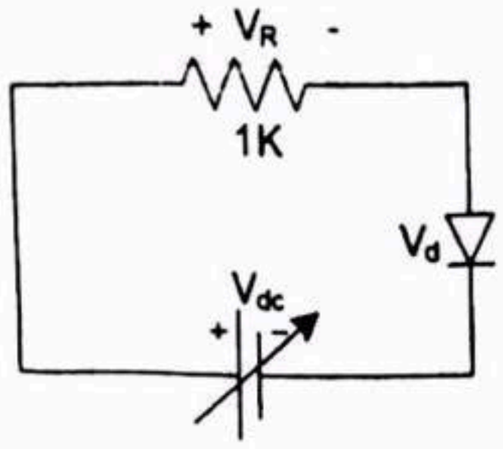


Figure 1.6 : Circuit Diagram for Obtaining Diode Diode Forward Characteristics.

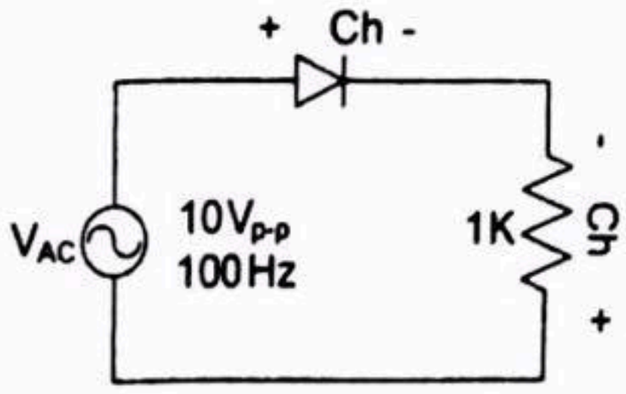


Figure 1.7 : Circuit Diagram for Obtaining Characteristics From Oscilloscope.

Procedure :

1. Measure the resistance accurately using multimeter.
2. Construct the circuit as shown in figure - 1.6.
3. Vary input voltage V_{dc}. Measure V_{dc}, V_d, V_R for the given values of V_d and record data on data table. Obtain maximum value of V_d without increasing V_{dc} beyond 25 volt.
4. Calculate the values of I_d using the formula, $I_d = V_R / R$.
5. Construct the circuit as shown in figure - 1.7.
6. Ste the oscilloscope in X-Y mode. Identify zero record on oscilloscope display. Make proper connection and observe the output.
7. Repeat the step 5 and 6 by increasing the input supply frequency 5 KHz.

Data Table :

V_{dc} (volt)	V_d (volt)	V_R (volt)	$I_d = V_R / R$ (mA)

Report :

1. Draw the I - V characteristics curve of diode from the reading obtain in this experiment.
2. Calculate static resistance for I_d = 5 mA and I_d = 10 mA.
3. Determine the Q- point for the circuit in figure - 6, when V_{dc} = 8 volt.

Experiment No: 02

Name of the Experiment: Diode rectifier circuits.

Objective:

Study of different diode rectifier circuits.

Theory:

A rectifier converts an AC signal into a DC signal. From the characteristic curve of a diode we observe that if allows the current to flow when it is in the forward bias only. In the reverse bias it remains open. So, when an alternating voltage (signal) is applied across a diode it allows only the half cycle (positive half cycle depending on the orientation of diode in the circuit) during its forward bias condition, other half cycle will be clipped off. In the output the load will get DC signal.

Diode rectifier can be categorized in two major types. They are -

1. Half-wave rectifier.
2. Full-wave rectifier.

Half - Wave Rectifier: Half-wave rectifier can be built by using a single diode. The circuit diagram and the wave shapes of the input and output voltage of half wave rectifier are shown bellow (figure 2.1) -

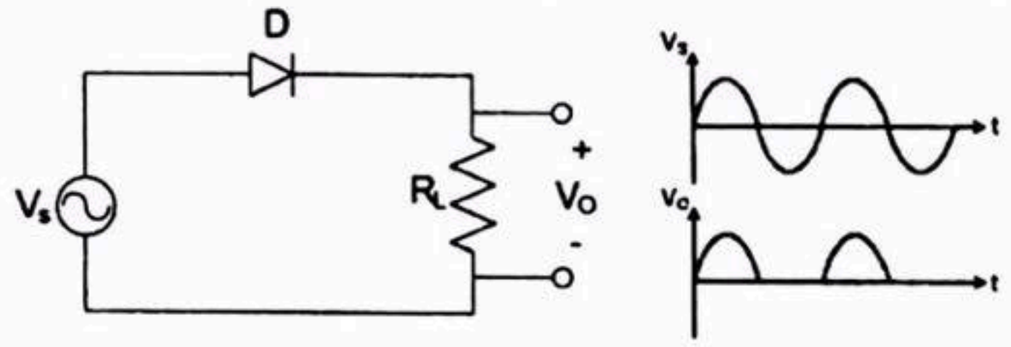


Figure 2.1: Half Wave Rectifier.

The major disadvantages of half wave rectifier are -

- In this circuit the load receives approximately half of input power.
- Average DC voltage is low.
- Due to the presence of ripple output voltage is not smooth one.

Full Wave Rectifier: in the full-wave rectifier both the half cycle is present in the output. Two circuits are used as full-wave rectifier are shown bellow -

a) Full-wave rectifier using center-tapped transformer.
b) Full-wave bridge rectifier.

Full-wave rectifier using center-tapped transformer: two diodes will be connected to the ends of the transformer and the load will be between the diode and center tap. The circuit diagram and the wave shapes are shown in bellow (figure 2.2) -

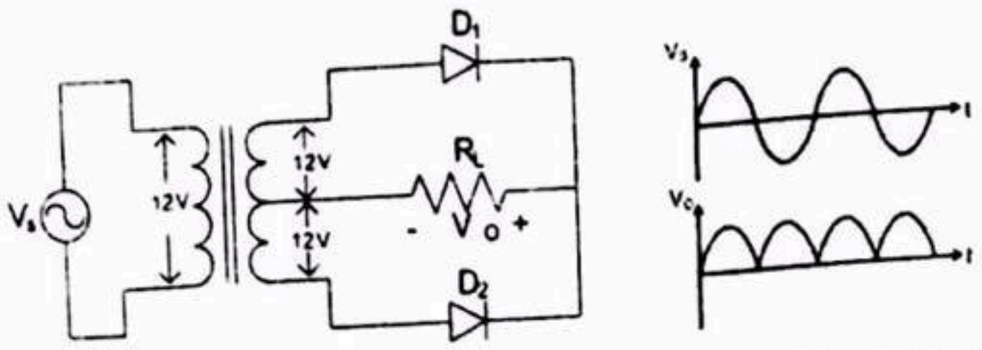


Figure 2.2: Full Wave Rectifier Using Center Tapped Transformer.

Full-wave rectifier using center-tapped transformer circuit has some advantages over full-wave rectifier. Those are -

- Wastage of power is less.
- Average DC output increase significantly.
- Wave shape becomes smoother.

The disadvantages of full-wave rectifier using center-tapped transformer are -

- Require more space and becomes bulky because of the transformer.
- Not cost effective (for using transformer).

Full-wave bridge rectifier: a bridge rectifier overcomes all the disadvantages of described above. Here four diodes will be connected as bridge connection. The circuit diagram and the wave shapes are shown in bellow (figure 2.3) -

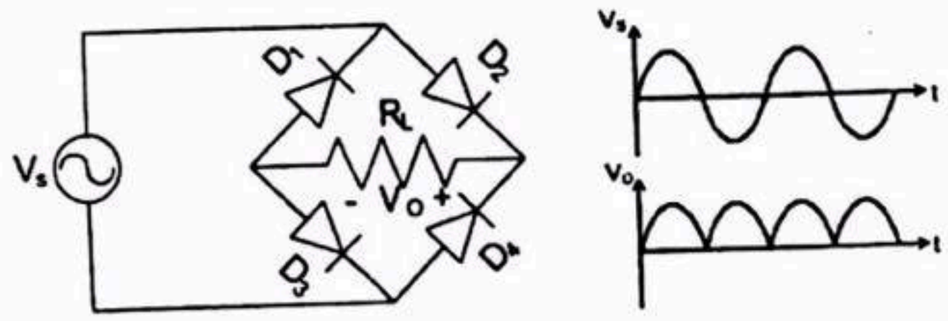


Figure 2.3: Full Wave Bridge Rectifier.

This rectifier however cannot produce a smooth DC voltage. It produces some ripple in the output. This ripple can be reducing by using filter capacitor across the load.

Equipments And Components:

Serial no.	Component Details	Specification	Quantity
1.	p-n junction diode	1N4007	4 piece
2.	Resistor	10KΩ	1 piece
3.	Capacitor	0.22μF, 10μF	1 piece each
4.	Signal generator		1 unit
5.	Trainer Board		1 unit
6.	Oscilloscope		1 unit
7.	Digital Multimeter		1 unit
8.	Chords and wire		as required

Experimental Setup:

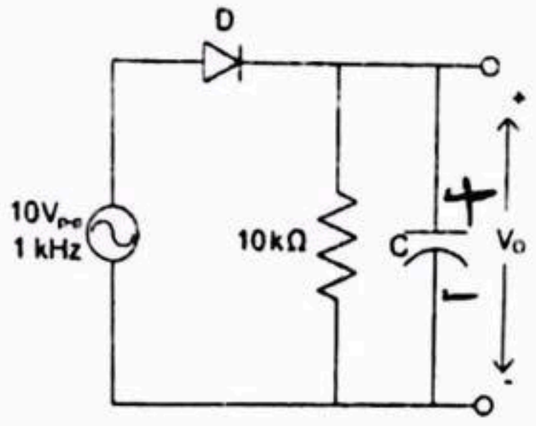


Figure 2.4 : Experimental Circuit 1.

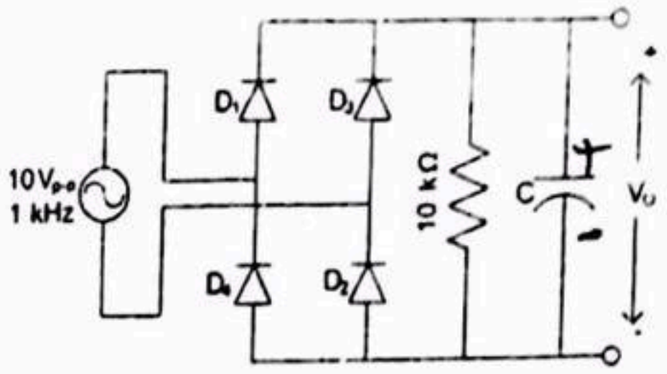


Figure 2.5 : Experimental Circuit 2.

Procedure:

1. Connect the circuit in breadboard as shown in figure 2.4 without capacitor.
2. Observe the output and input voltages in the oscilloscope and draw them.
3. Connect the 0.22μF capacitor and repeat step 2.
4. Connect the 10μF capacitor and repeat step 2. How does the output wave-shape differ from that in step 3?
5. Vary the frequency from 10 KHz to 100 Hz. What effects do you observe when frequency is changed?
6. Connect the circuit breadboard as shown in figure 2.5 without capacitor.
7. Observe the output and input voltages in the oscilloscope and draw them.
8. Connect the 0.22μF capacitor and repeat step 7.
9. Connect the 10μF capacitor and repeat step 7. How does the output wave-shape differ from that in step 8?
10. Vary the frequency from 10 KHz to 100 Hz. What effects do you observe when frequency is changed?

Report:

1. Write the answers that were asked during the working procedure.
2. Draw the input wave, output wave (without and with capacitor) for both the circuits.
3. What is the effect in output for changing input signal frequency for both the circuits (without and with capacitor)?
4. What is the function of capacitor in the both circuits? Why a capacitor of higher value is preferable?

Experiment No : 04

Name of the Experiment : Zener Diode applications.

Objective:

Study of the Zener Diode applications.

Theory :

The diodes we have studied before do not operate in the breakdown region because this may damage them. A Zener diode is different; it is a silicon diode that the manufacturer has optimized for operation in the breakdown region. It is used to build voltage regulator circuits that circuits that hold the load voltage almost constant despite large change in line voltage and load resistance. The symbol of Zener diode shows in figure 4.1.

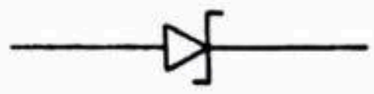


Figure 4.1 : Symbol of Zener Diode.

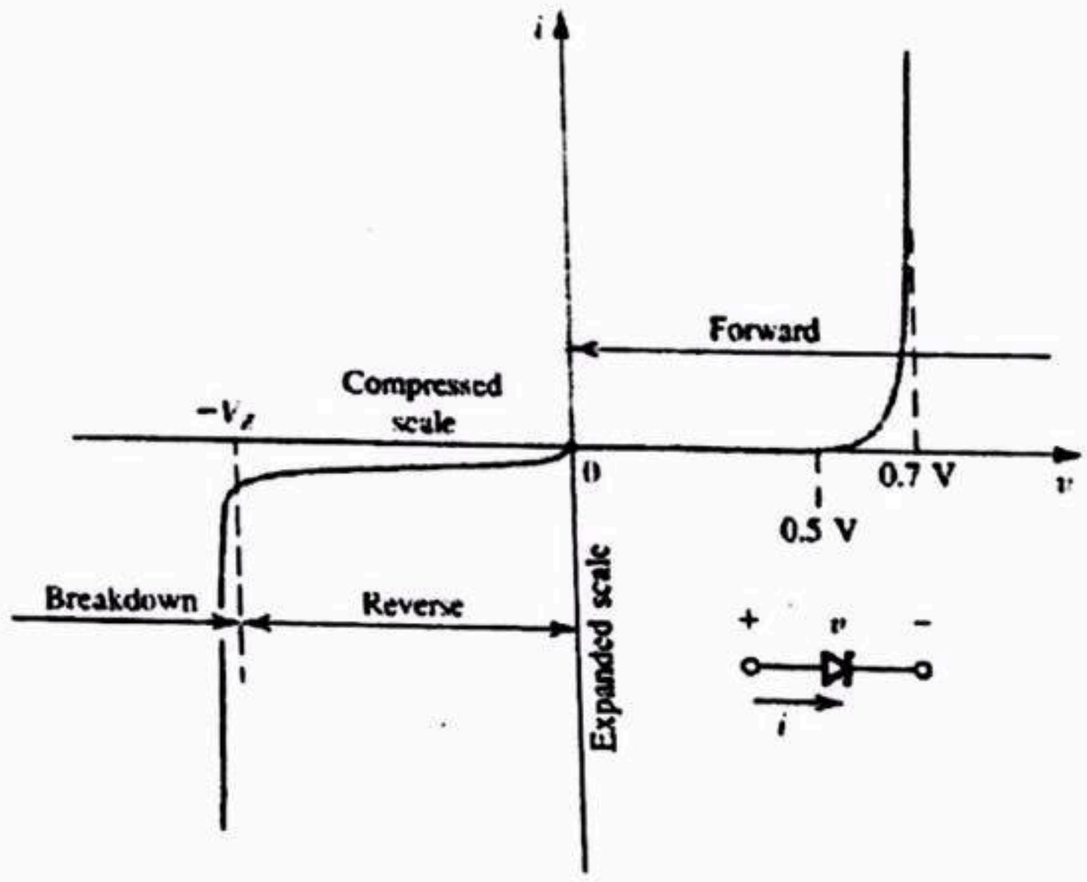


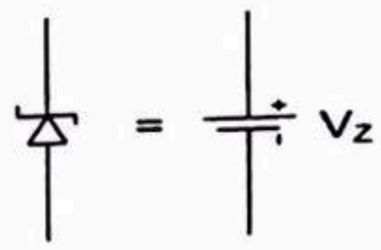
Figure 4.2 : I - V Characteristics of Zener Diode.

The Zener diode may have a breakdown voltage from about 2 to 200 volts. These diodes can operate in any of three regions – forward, leakage and breakdown. Figure 4.2 shows the I-V characteristics curve of Zener diode.

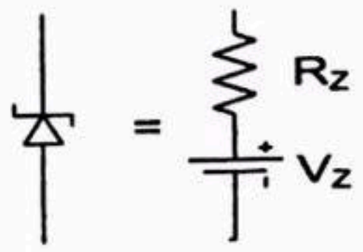
- In the forward region it works as an ordinary diode.
- In the leakage region (between zero and breakdown) it has only a small reverse saturation current.
- In the breakdown it has a sharp knee, followed by an almost vertical increase in current without changing the voltage.
- The voltage is almost constant, approximately equal to V_z over most of the breakdown region.

Equivalent circuits of Zener Diode : Two approximation are used for Zener Diode equivalent circuit.

First Approximation : As the voltage remains constant across the Zener diode though the current changes through it, it is considered as a constant voltage source according to the first approximation.



Second Approximation : A Zener resistance is in series with the ideal voltage source is approximated.



Equipments and Components:

Serial no.	Component Details	Specification	Quantity
1.	Zener diode	5 volts	1 piece
2.	Resistor	220Ω, 470Ω, 1KΩ	1 piece each
3.	POT	10KΩ	1 unit
4.	Trainer Board		1 unit
5.	DC Power Supply		1 unit
6.	Digital Multimeter		1 unit
7.	Chords and wire		as required

Experimental Setup:

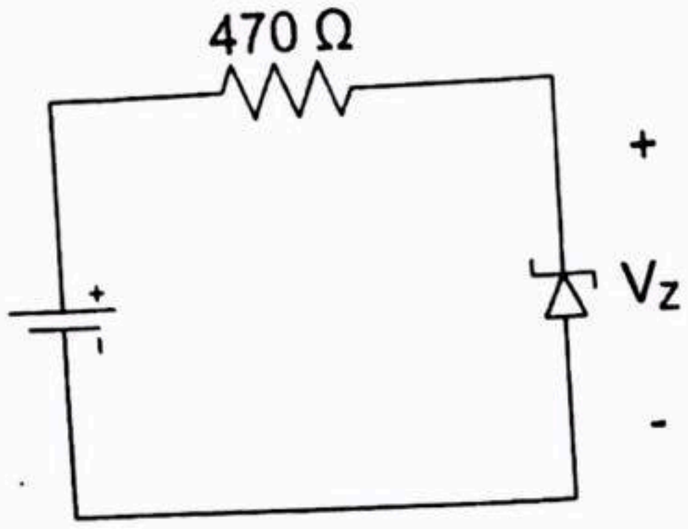


Figure 4.3 : Experimental Circuit 1.

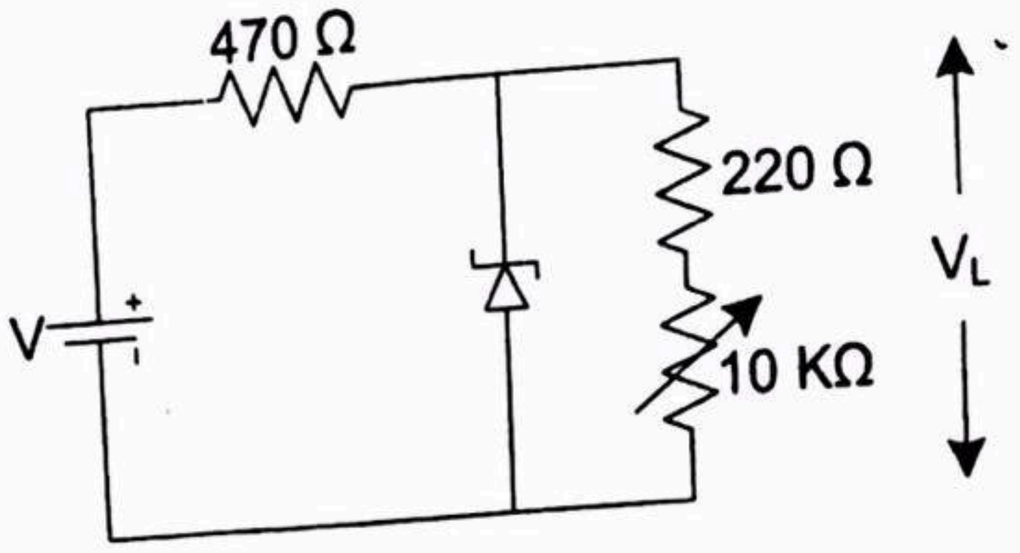


Figure 4.4 : Experimental Circuit 2.

Procedure :

1. Connect the circuit as shown in the figure 4.3
2. Vary the supply voltage from zero volt, complete the Table 4.1.
3. Connect the circuit as shown in the figure 4.4
4. Keep the POT at maximum position and power up the circuit. Apply 10 as V.
5. Gradually decrease the POT resistance and complete the Table 4.2.
6. Replace load with 1KΩ resistance, vary the supply voltage and take reading for Table 4.3.

Table 4.1 : Data for I - V characteristics.

V (volts)	V_R (volts)	V_z (volts)	$I_z = V_R / R$ (mA)
1.0			
2.0			
3.0			
4.0			
5.0			
6.0			
7.0			
8.0			
9.0			
10.0			
11.0			
12.0			

Table 4.2 : Data for regulation due to load variation.

V_{220} (mV)	V_L (volts)	I_L (Amp)

Table 4.3 : Data for regulation due supply voltage variation.

V (volts)	V_L (volts)
5.0	
6.0	
7.0	
8.0	
9.0	
10.0	
11.0	
12.0	

Report :

1. Plot the I - V characteristics of Zener diode. Determine the Zener breakdown voltage from the plot.
2. Plot I_L vs V_L for the data table 4.2. Find the voltage regulation.
3. Plot V_L vs V for the data table 4.3. Find the voltage regulation.

Experiment No: 05

Name of the Experiment : The output characteristics of CE (common emitter) configuration of BJT.

Objective:

Study of the output characteristics of CE (common emitter) configuration of BJT.

Theory :

Unlike the diode, which has two doped region, a transistor has three doped region. They are as follows –

a) Emitter,
b) Base and
c) Collector.

These three doped regions form two junctions: One between the emitter and base and other between the collector and the base. Because of these it can be thought as combination of two diodes, the emitter and the base form one diode and the collector and base form another diode. The emitter is heavily doped. Its job is to emit or inject free majority carrier (electron for NPN and hole for PNP) into the base. The base is lightly doped and very thin. It passes the most of the emitter-injected electron (for NPN) into the collector. The doping level of the collector is between emitter and base. Figure 5.1 shows the biased NPN transistor.

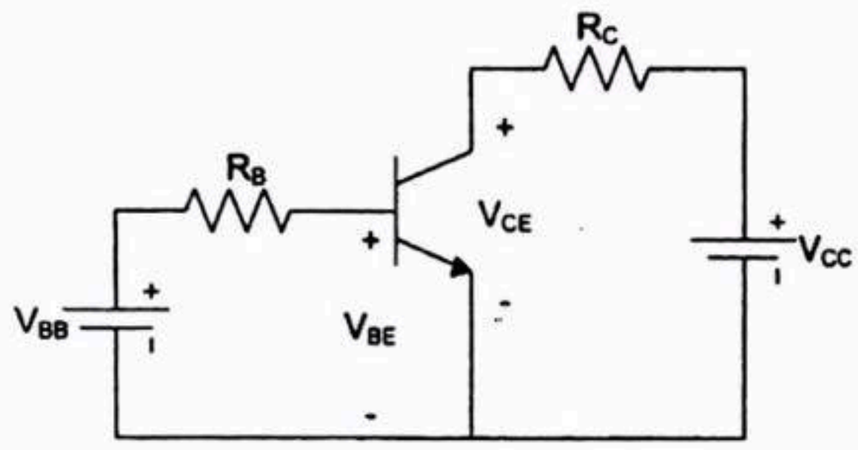


Figure 5.1 : Biasing of an NPN transistor.

If the V_{BB} is greater than the barrier potential, emitter electron will enter base region. The free electron can flow either into the base or into the collector. As base lightly doped and thin, most of the free electron will enter into the collector.
There are three different current in a transistor. They are emitter current (I_E), collector current (I_C) and the base current (I_B) are shows in figure 5.2.

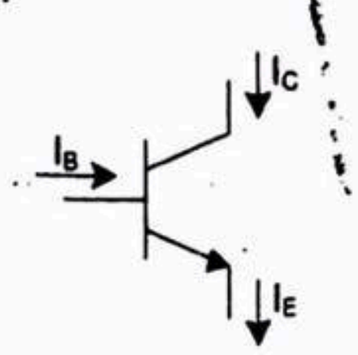


Figure 5.2 : Different current in transistor.

Here, $I_E = I_C + I_B$, and the current gain $\beta = \frac{I_C}{I_B}$

Characteristics Curve : The characteristics of a transistor is measured by two characteristics curve. They are as follows –

a) Input characteristics curve.
b) Output characteristics curve.

Input Characteristics Curve : Input characteristics is defined as the set of curves between input current (I_B) vs. input voltage (V_{BE}) for the constant output voltage (V_{CE}). It is the same curve that is found for a forward biased diode.

Output Characteristics Curve : Output characteristics is defined by the set of curves between output current (I_C) vs. output voltage (V_{CE}) for the constant input current (I_B). The curve has the following features –

- It has three regions namely Saturation, Active and Cutoff region.
- The rising part of the curve, where V_{CE} is between 0 and approximately 1 volt is called saturation region. In this region the collector diode is not reversed biased.
- When the collector diode of the transistor becomes reverse biased, the graph becomes horizontal. In this region the collector remains almost constant. This region is known as the active region. In applications where the transistor amplifies weak radio and TV signal, it will always be operation in the active region.
- When the base current is zero, but there is some collector current. This region of the transistor curve is known as the cutoff region. The small collector current is called collector cutoff current.
- For different value of base current (I_B) an individual curve can be obtained.

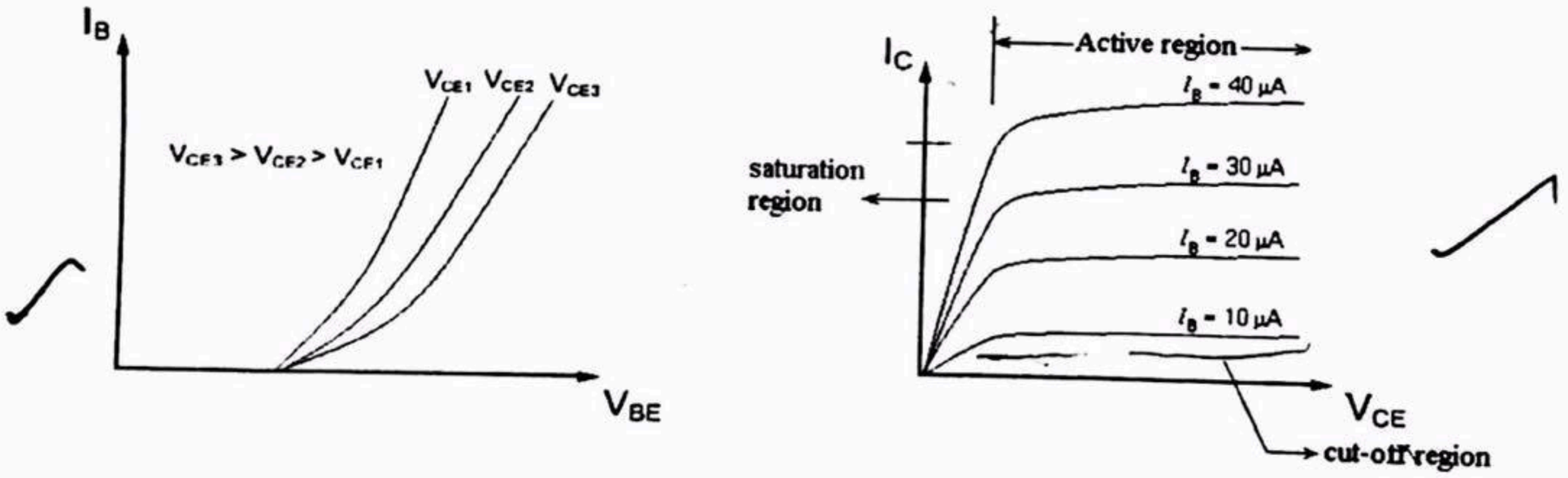


Figure 5.3 : (a) Input Characteristic, (b) Output Characteristic of NPN transistor.

Equipments And Components:

Serial no.	Component Details	Specification	Quantity
1.	Transistor	C828	1 piece
2.	Resistor	470Ω, 2.2KΩ, 3.3KΩ, 4.7KΩ, 10KΩ, 470KΩ	1 piece each
3.	POT	100KΩ	1 unit
4.	Trainer Board		1 unit
5.	DC Power Supply		1 unit
6.	Digital Multimeter		1 unit
7.	Chords and wire		as required

Experimental Setup:

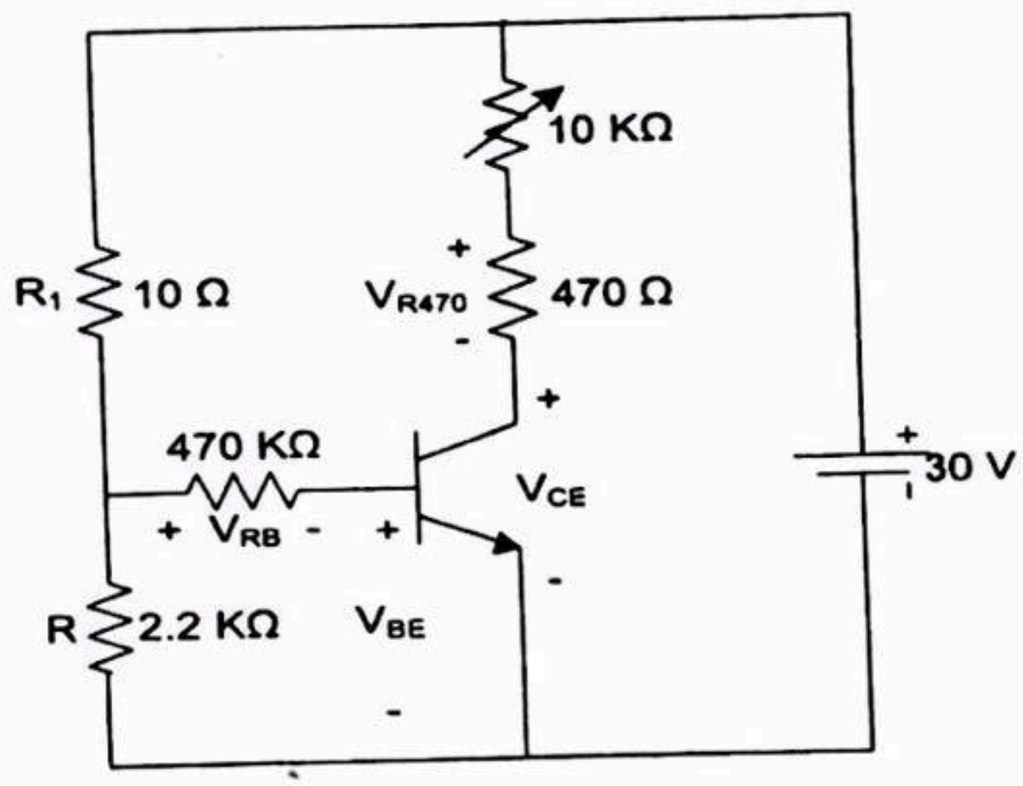


Figure 5.4: Experimental Circuit.

Procedure:

1. Connect the circuit as shown in the figure 5.4. Use 2.2 KΩ as R.
2. Measure V_{RB} and calculate I_S using $I_E = V_{RB} / R_B$. (We will assume that I_B to be constant for a particular setup at input.)
3. Measure the voltages of V_{CE} and V_{R470}. And calculate I_C using $I_C = V_{R470} / R_{470}$.

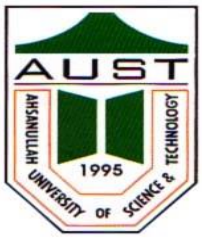
4. Take at least 10 reading by varying the POT.
5. Repeat step 1 to 4 with resistance R as 3.3 KΩ and 4.7 KΩ.

Table 5.1 : Data for I - V characteristics of transistor.

R (KΩ)	$I_B = V_{RB} / R_B$ (μA)	V_{CE} (volts)	V_{R470} (volts)	$I_C = V_{R470} / R_{470}$ (mA)
2.2				
3.3				
4.7				

Report:

1. Plot the graph of I_C vs. V_{CE} with necessary details. Show the different regions of operation.
2. Plot a hypothetical output characteristic using PNP transistor.
3. Find β for the three different condition.



Ahsanullah University of Science and Technology (AUST)
Department of Mechanical and Production Engineering

LABORATORY MANUAL

For the students of

Department of Mechanical and Production Engineering

2nd Year, 2nd Semester

Student Name :

Student ID :

Ahsanullah University of Science and Technology

Department of Electrical and Electronic Engineering

LABORATORY MANUAL

FOR

ELECTRICAL AND ELECTRONIC SESSIONAL COURSES

Student Name :

Student ID :

Course no : EEE 3104

Course Title: Digital Electronics-I Laboratory

For the students of

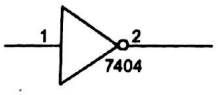
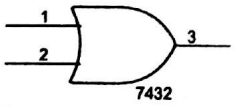
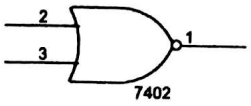
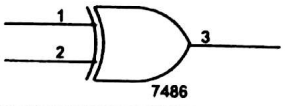
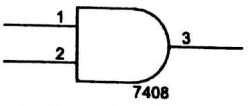
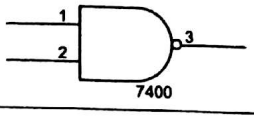
Department of Electrical and Electronic Engineering

3rd Year, 1st Semester

Experiment: 1
Experiment name: *Introduction to different digital ICs.*

Introduction:
In this experiment you will be introduced to different digital ICs that will be used in this digital lab to perform different functions and also the function of each IC. You are asked to memorize the followings associated with each IC.

1. IC number
2. IC name
3. Total number of pins
4. V_{cc} pin number
5. Ground pin number

IC number	IC name	Schematic view
7404	NOT	
7432	OR	
7402	NOR	
7486	XOR	
7408	AND	
7400	NAND	

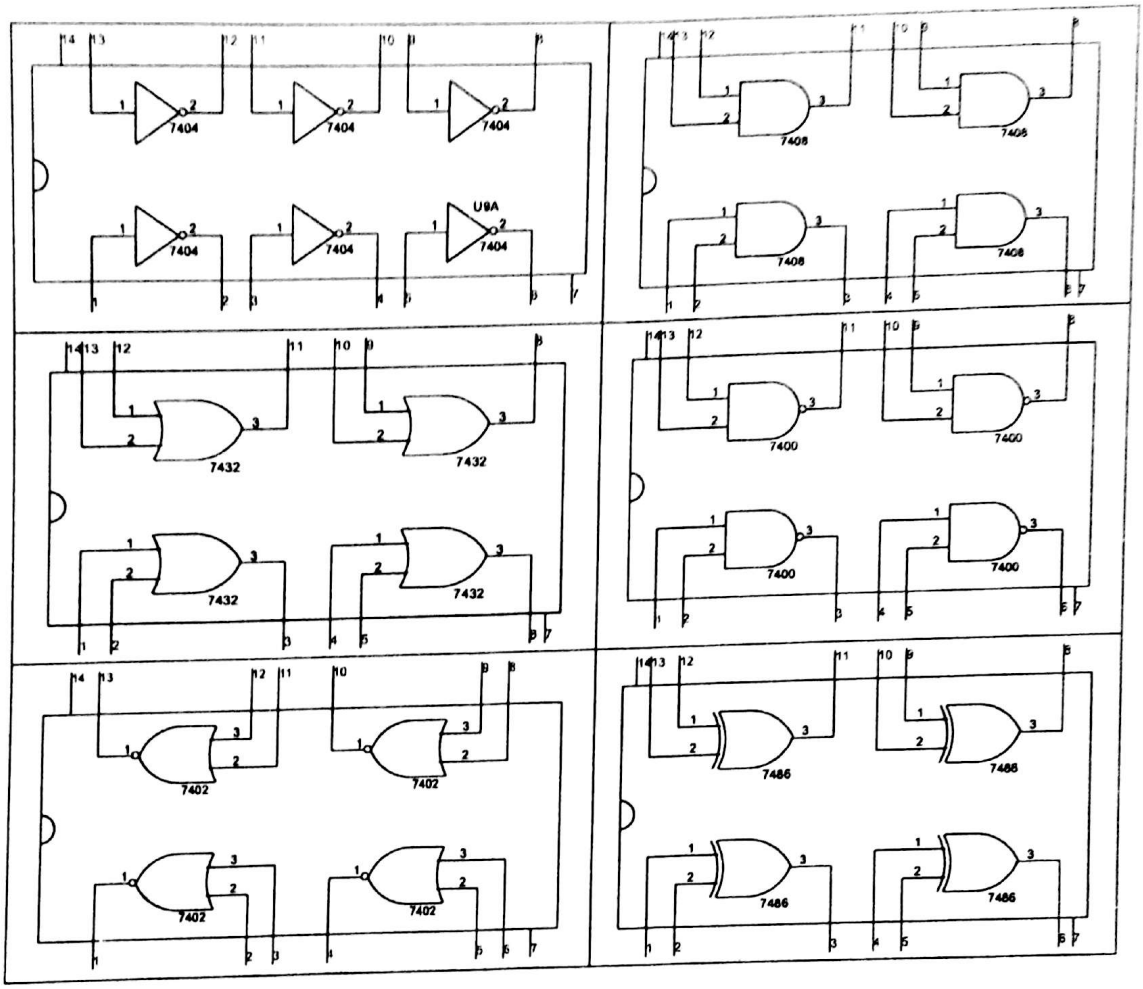
Equipment:

1. Trainer Board
1. IC 7400,7402,7404,7408,7432,7486
2. Microprocessor Data handbook

Procedure:

1. Take any of the ICs. From microprocessor data handbook find the name of the IC, total number of pins that it has, V_{cc} pin and ground pin.

IC Number	IC name	Total number of pin	V_{cc} pin no.	Ground pin no.
7400	NAND	14	14	7
7402	NOR	14	14	7
7404	NOT	14	14	7
7408	AND	14	14	7
7432	OR	14	14	7
7486	XOR	14	14	7



1. Note the number of gates each IC has from the handbook.
2. Now fill up the following table.

Input A	Input B	7400 NOT $Y = \overline{A}$	7432 OR $Y = A + B$	7402 NOR $Y = \overline{A + B}$	7486 XOR $Y = A \oplus B$	7408 AND $Y = AB$	7400 NAND $Y = \overline{AB}$
0	0						
0	1						
1	0						
1	1						

3. Now verify the observed output with the desired output for different combination of inputs.
4. Repeat step 1 to 4 for different ICs.

Assignment:

1. How can you make a three input AND/OR/XOR gate with a two input AND/OR/XOR gate?
2. Is it possible to make a three input NAND/NOR gate with a two input NAND/OR gate? Justify your answer.

Experiment: 2
Experiment name: *Introduction to Combinational logic.*

Introduction:
Logic design basically means the construction of appropriate function, presented in Boolean algebraic form, then edification of the logic diagram, and finally choosing of available ICs and implementing the IC connection so that the logic intended is achieved. The efficiency in simplifying the algebra leads to less complicated logic diagram, which in the end leads to easier IC selection and easier circuit implementation.

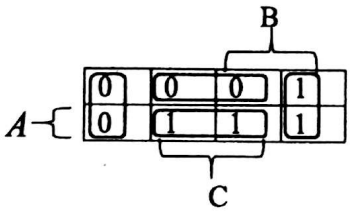
Caution:
1. Remember to properly identify the pin numbers so that no accidents occur.
2. Properly bias the ICs appropriate voltages to appropriate pins.

Equipment:
1. Trainer Board
2. IC 7400,7402,7404,7408,7432,7486
3. Microprocessor Data handbook

Job 1:

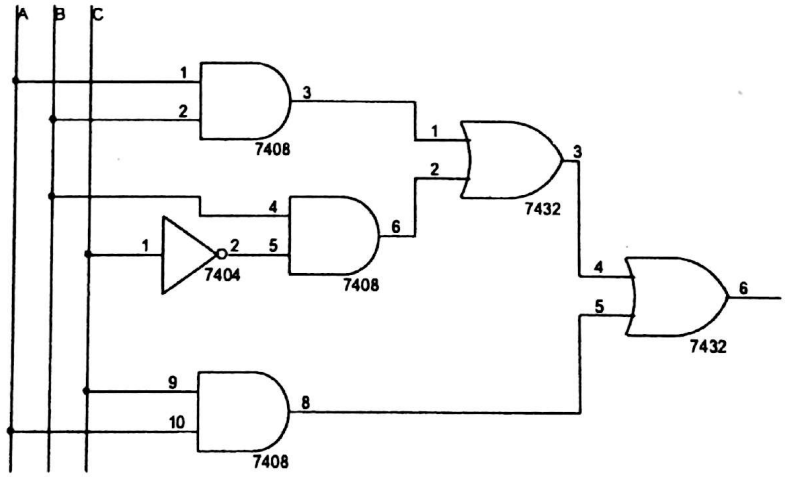
Implement of function $f = AB + BC' + CA$

$$= ABC + ABC' + ABC' + A'BC' + ABC + AB'C$$
$$= ABC + ABC' + A'BC' + AB'C$$
$$= m_7 + m_6 + m_2 + m_5$$



$F = AC + BC'$
$= SOP$

$F' = B'C' + A'C$
$\Rightarrow F = (B'C' + A'C)'$
$\Rightarrow F = (B + C)(A + C')$



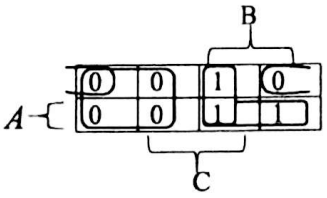
Procedure:
1. Draw logic diagram to implement the function.
2. Select ICs from the equipment list.

3. Note the output logic for all combination of inputs.
4. Now fill up the truth table for that function.
5. Simplify the function in POS and in SOP form using K-map.
6. Repeat step-1, 2 and 3.

Job 2:

Implement of function $f = (AB + B)(C + A)(AC + B)$

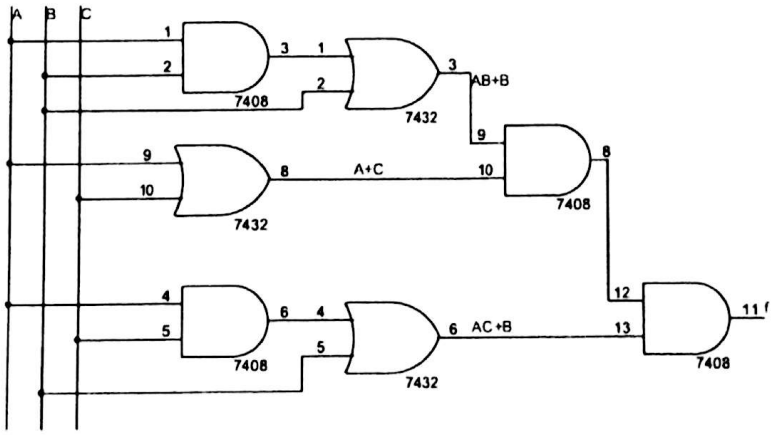
$$= B(A + B)(A + C)(A + B)(B + C)$$
$$= B(A + B)(A + C)(B + C)$$
$$= B(AA')(A + B)(A + C)(B + C)$$
$$= (A + B)(A' + B)(A + C)(B + C)$$
$$= (A+B+C)(A+B+C')(A'+B+C)(A+B+C')(A+B+C)(A+B'+C)(A+B+C)(A'+B+C)$$
$$= (A + B + C)(A + B + C')(A' + B + C)(A' + B + C')(A + B' + C)$$
$$= M_0 M_1 M_4 M_2 M_5$$



$F = AB + BC$

$F' = B' + A'C'$

$\Rightarrow F = B(A + C)$



Procedure:

1. Simplify the function in POS form and in SOP form by using Boolean algebra.
2. Draw logic diagram to implement the function.
3. Select ICs from the equipment list.
4. Note the output logic for all combination of inputs.

Experiment: 3
Experiment name: *Construction of adders and sub tractors using basic logic gates.*

Introduction:
Adders and sub tractors are the basic operational units of simple digital arithmetic operations. In this experiment, the students will construct the basic adder and sub tractor circuit with common logic gates and test their operability. Then in the last job, they will cascade adder ICs to get higher bit adders.

Caution:
1. Remember to properly identify the pin numbers so that no accidents occur.
2. Properly bias the ICs with appropriate pins.

Equipment:
1. Trainer Board
2. IC 7400, 7402, 7404, 7408, 7432, 7486
3. Microprocessor Data handbook

Job 1:
Implementation of a half adder and a half sub tractor.

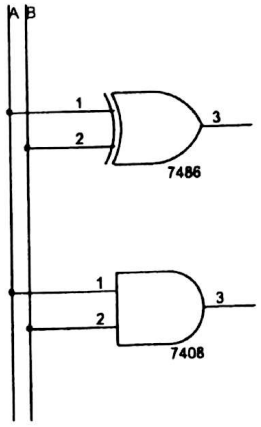


Fig: Half Adder

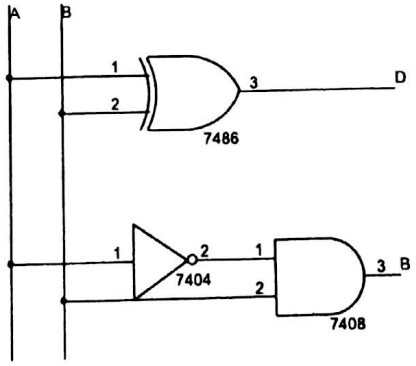


Fig: Half sub tractor

Procedure:
1. Fill up the truth table for a half adder.

A	B	C	S

$S = A \oplus B$
$C = AB$

2. Determine the Boolean function for a half adder.
3. Construct the logic diagram from the Boolean functions.
4. Select the ICs from the equipment list.
5. Implement the output logic and compare with step-1.
6. Repeat the whole procedure for half a sub tractor.

A	B	B	D

$D = A \oplus B$
$B = A'B$

Job 2:

Implement of a full adder and a full sub tractor.

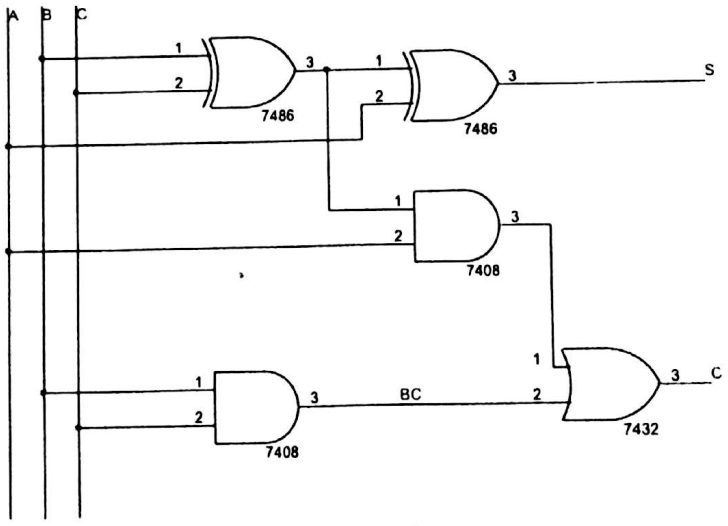


Fig: full adder

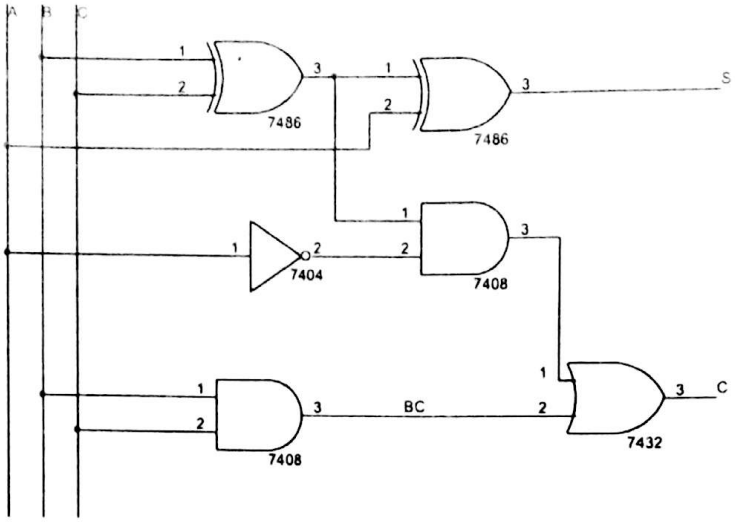


Fig: full subtractor

Procedure:

1. Fill up the truth table for a full adder.

A	B	C	C	S
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

$S = A'B'C + A'BC' + AB'C' + ABC$

$\Rightarrow S = A \oplus B \oplus C$

$C = A'BC + AB'C + ABC' + ABC$

$\Rightarrow C = BC + A(B \oplus C)$

2. Determine the Boolean function for a full adder.
3. Construct the logic diagram from the Boolean functions.
4. Select the ICs from the equipment list.
5. Implement the output logic and compare with step-1.
6. Repeat the whole procedure for a full sub tractor.
7. Now draw a full adder using two half adder block and basic gates.
8. Repeat step-7 for a full sub tractor.

A	B	C	B	D
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

$S = A'B'C + A'BC' + AB'C' + ABC$

$\Rightarrow S = A \oplus B \oplus C = D$

$C = A'BC + AB'C + ABC' + ABC$

$\Rightarrow C = BC + A'(B \oplus C)$

Experiment: 4

Experiment name: *Design a Combinational circuit that will act as an Adder if control bit is '0' and as a sub tractor if control bit is '1'.*

Introduction:

Addition of two 4-bit binary numbers can be easily done using a 4-bit binary adder IC (7483/74283). Taking the 2's complement of the subtrahend and then adding that with the minuend can do subtraction of two 4-bit binary numbers.

Caution:

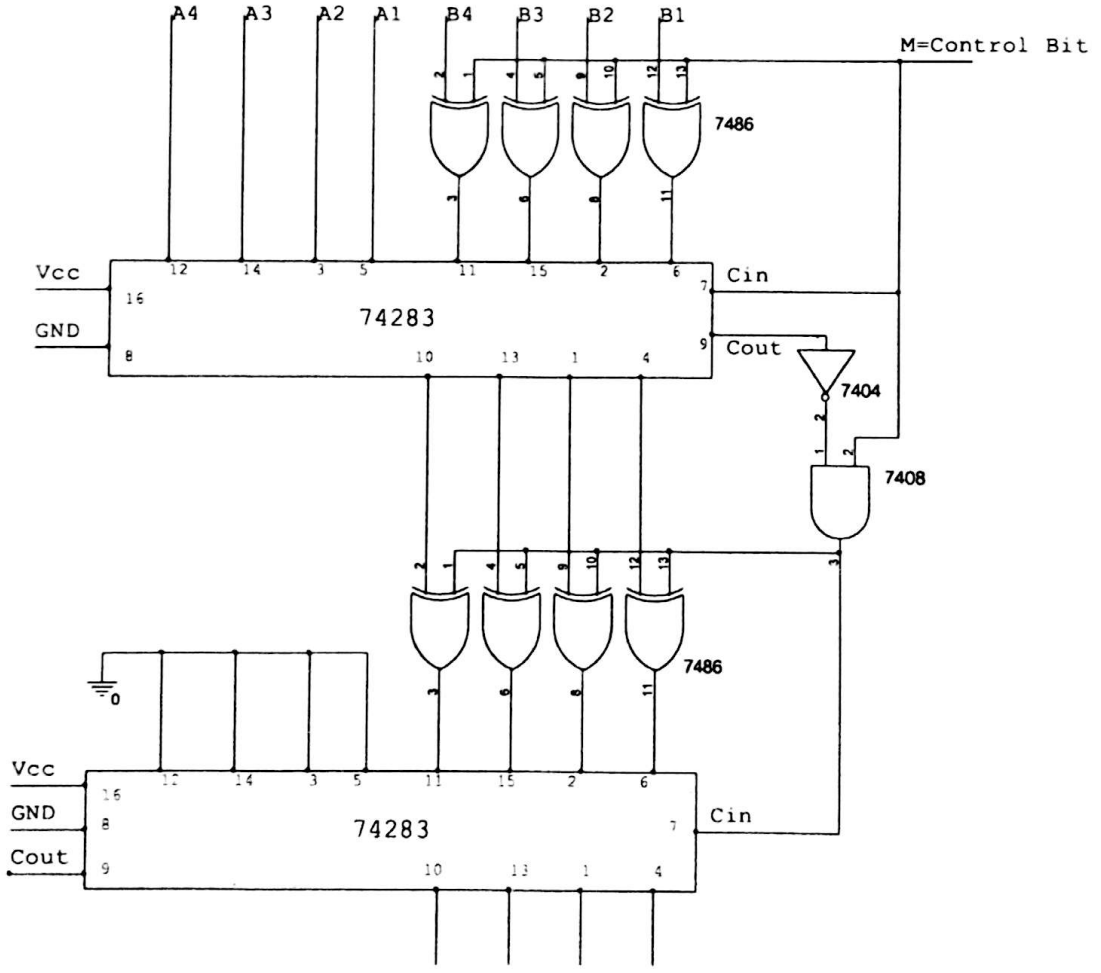
1. Remember to properly identify the pin numbers so that no accidents occur.
2. Properly bias the ICs with appropriate voltages to appropriate pins.

Equipment:

1. Trainer Board
2. IC 74283,7408,7432,7486.
3. Microprocessor Data handbook

Procedure:

1. Draw the logic diagram to implement the task.



2. Select the required ICs.
3. Note the output logic for different inputs.

A	*B*	*S*	Output
0001	0010	0	
0001	0010	1	
1001	0011	0	
1011	0111	1	
1011	0111	0	
1100	1001	1	
1111	1111	0	
1111	1111	1	

Experiment: 5

Experiment name: *Design a BCD adder that will add two BCD numbers and the sum will be also in BCD.*

Introduction:

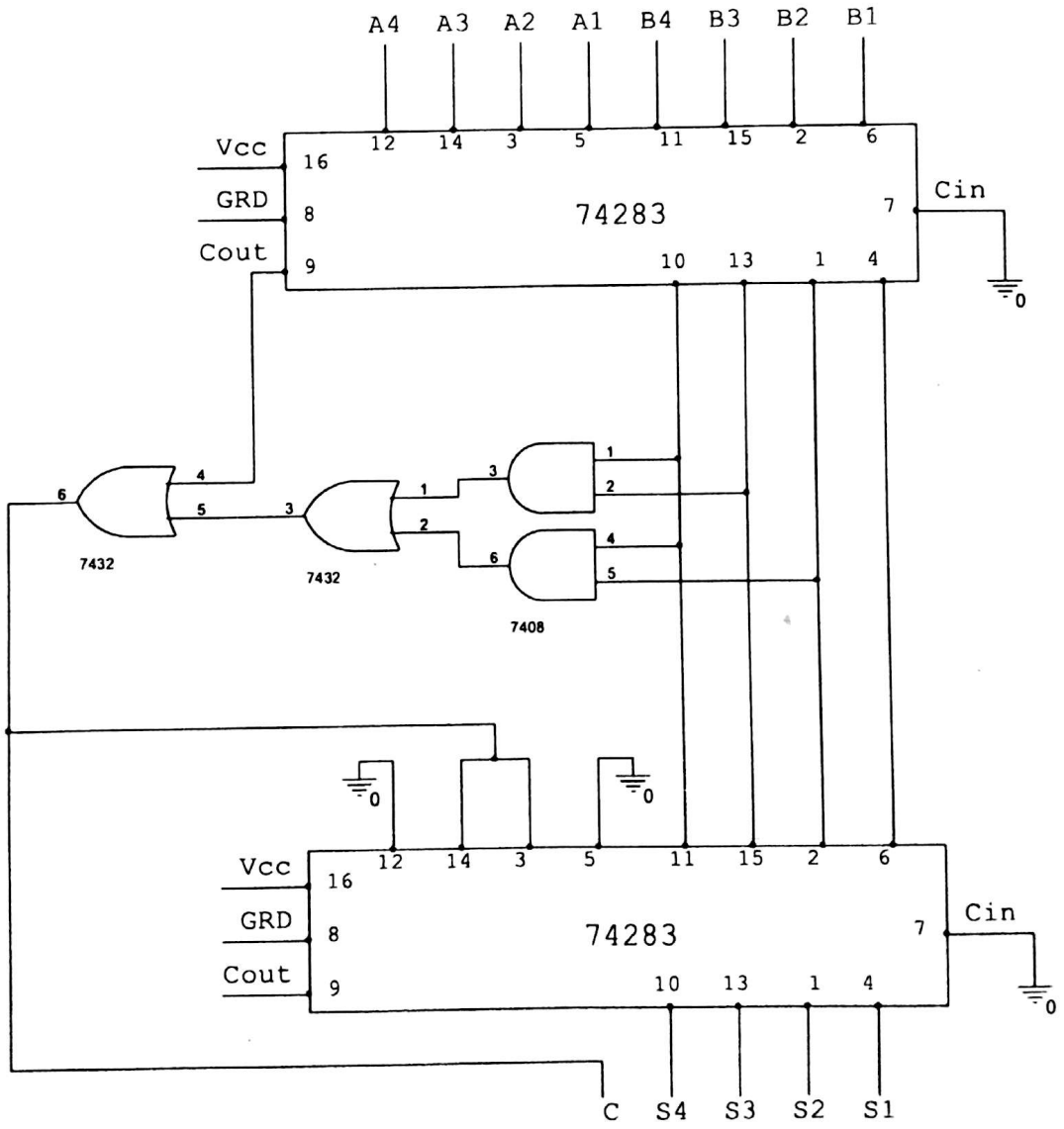
A BCD adder can be designed by considering the arithmetic addition of two decimal digits in BCD, together with a possible carry from a previous stage. Since each input digit does not exceed 9, the output sum cannot be greater than 9+9+1=19. This can be designed with a 4-bit binary adder together with a correction logic circuit.

Caution:

1. Remember to properly identify the pin numbers so that no accidents occur.
2. Properly bias the ICs with appropriate voltages to appropriate pins.

Procedure:

1. Draw the logic diagram to implement the task.



2. Select the required ICs.
3. Fill up the following truth table for 19 inputs.

	Binary Sum					BCD Sum				
Decimal	K	Z_8	Z_4	Z_2	Z_1	C	S_8	S_4	S_2	S_1
0										
1										
2										
3										
4										
5										
6										
7										
8										
9										
10										
11										
12										
13										
14										
15										
16										
17										
18										
19										

Experiment: 6
Experiment name: *Introduction to Multiplexers.*

Introduction:
Multiplexers are the most important attributions of digital circuitry in communication hardware. These digital switches enable us to achieve the communication network we have today. In this experiment the students will have to construct MUX (as they call multiplexers) with simple logic gates and they will implement general logic using 8:1 MUX as the basic constructional unit.

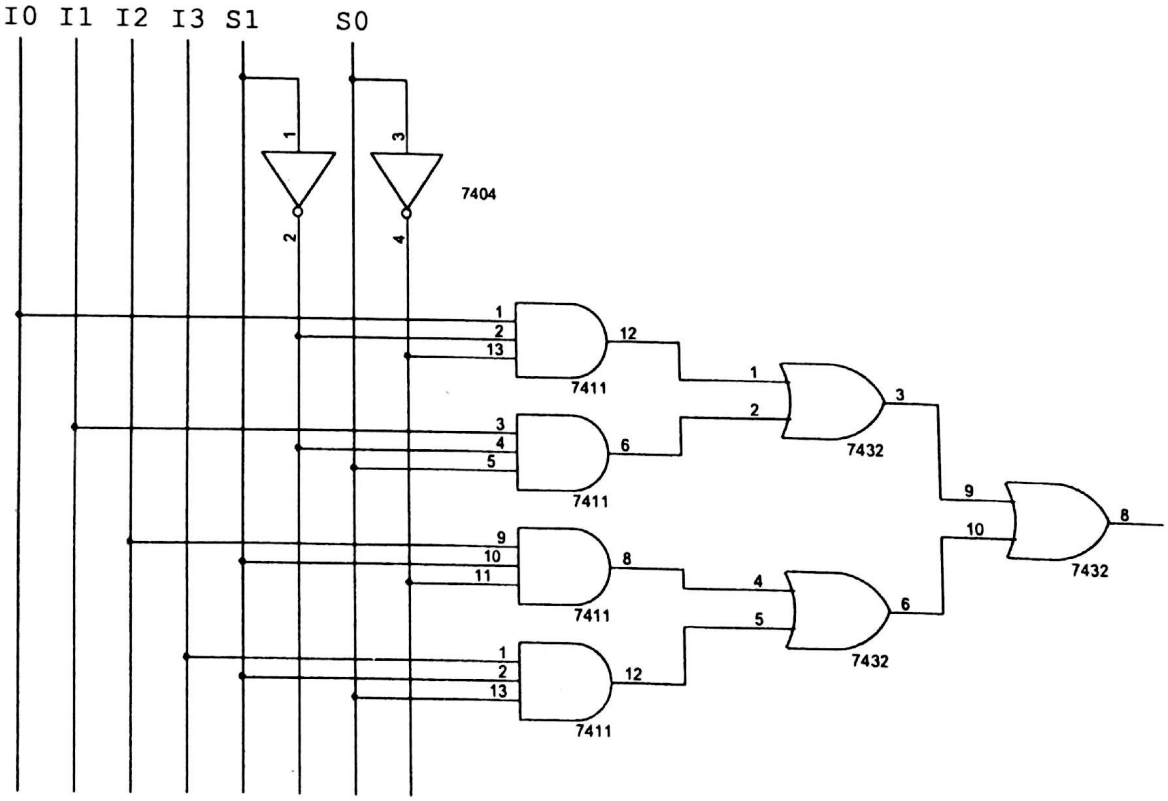
Caution:
1. Remember to properly identify the pin numbers so that no accidents occur.
2. Properly bias the ICs with appropriate voltages to appropriate pins.

Equipment:
1. Trainer Board
2. IC 74151, 7432, 7408, 7404
3. Microprocessor Data handbook.

Job 1:

Implementation of a four to one way Multiplexer, (4:1 MUX) with basic gates.

Procedure:
1. Write the truth table for four to one way MUX.
2. Write the Boolean function for the output logic.
3. Draw the logic diagram to implement the Boolean function.



4. Select ICs from the equipment list.
5. Observe and note the output logic for all combination of inputs.

Job 2:

Implement the following function using an 8:1 MUX.

$$F(A,B,C,D)=\sum(0,1,3,5,8,9,14,15)$$

Procedure:

1. Write the truth table for the above function.

	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7
A'								
A								

2. Draw the logic diagram to implement the Boolean function.

A	B	C	D	Y

3. Select ICs from the equipment list.
4. Observe and note the output logic for all combination of inputs.

Assignment:

1. Implement a Full Adder using an 8:1 MUX.
2. Repeat 1 using two 4:1 MUX and basic gates.
3. How can you implement a 4:1 MUX using only three 2:1 MUX?

Experiment: 7
Experiment name: *Implementation of Demultiplexers and Priority Encoders.*

Introduction:

A Demultiplexer does the opposite function of multiplexers. It has one input line and 2^n output lines, where n is the number of selection bits. The output channel can be selected depending on the combination of selection bits. An encoder has 2^n input lines and n output line. A priority encoder is designed to give output for lowest/highest input lines. For example, If D3, D2 and D1 lines have '1' as in their inputs, the output would be '11' as priority is given to highest input line.

Caution:

1. Remember to properly identify the pin numbers so that no accidents occur.
2. Properly bias the ICs with appropriate voltages to appropriate pins.

Equipment:

1. Trainer Board
2. IC 7432, 7408, 7404
3. Microprocessor Data handbook.

Job 1:

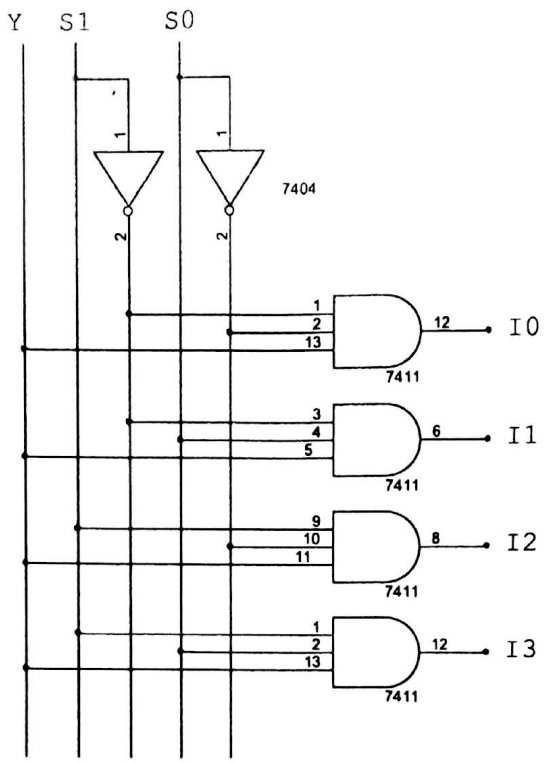
Implementation of a one to four way Demultiplexer, (1:4 DEMUX) with basic gates.

Procedure:

1. Write the truth table for one to four way DEMUX.

S_1	S_0	I_0	I_1	I_2	I_3

2. Write the Boolean function for the output logic.
3. Draw the logic diagram to implement the Boolean function.



4. Select ICs from the equipment list.
5. Observe and note the output logic for all combination of inputs.

Job 2:

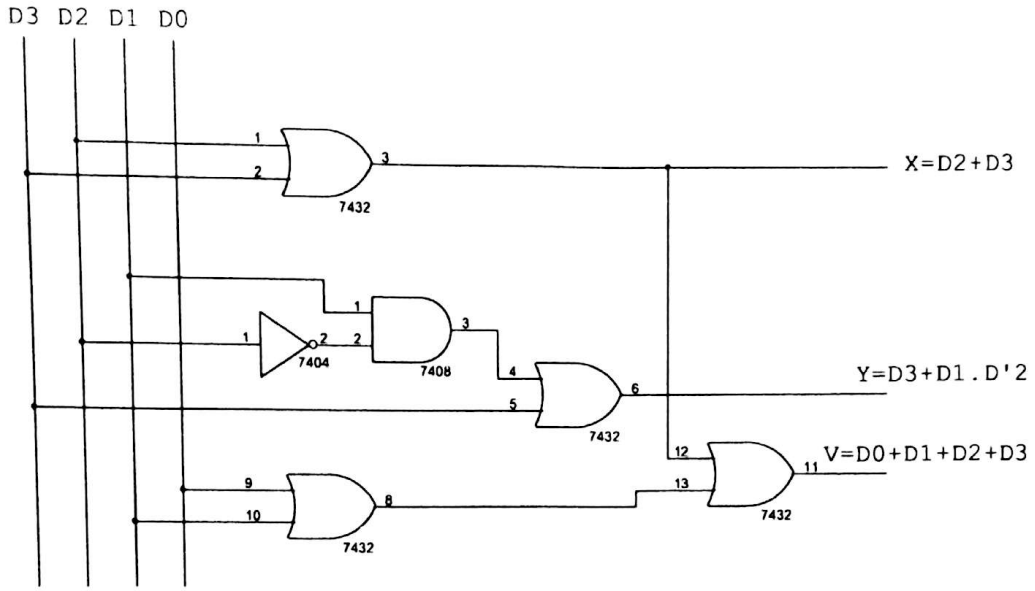
Implement a 4×2 *priority encoder with basic gates.*

Procedure:

1. Write the truth table for 4×2 priority encoder.

D_3	D_2	D_1	D_0	X	Y	V

2. Write the Boolean function for the output logic.
3. Simplify the Boolean function using K-map.
4. Draw the logic diagram to implement the simplified Boolean function.



5. Select ICs from the equipment list.
6. Observe and note the output logic for all combination of inputs.

Experiment: 8
Experiment name: *Design of Flip-flop using basic gates.*

Caution:

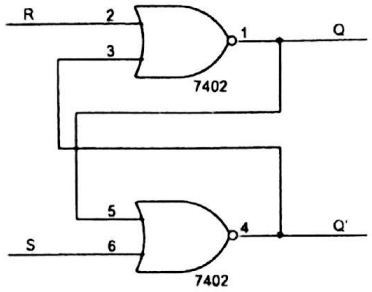
1. Remember to properly identify the pin numbers so that no accidents occur.
2. Properly bias the ICs with appropriate voltages to appropriate pins.

Equipment:

1. Trainer Board
2. IC 7400, 7402, 7432, 7408, 7404
3. Microprocessor Data handbook

Job 1:

Design of an SR Flip-flop using NOR gates only.



Procedure:

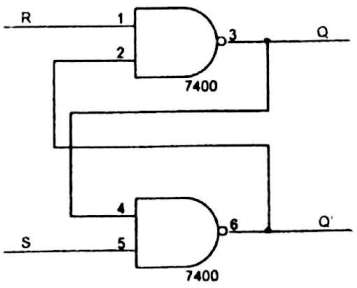
1. Draw the logic diagram to implement SR Flip-flop.
2. Fill up the table with different combination of inputs.

S	*R*	*Q*	*Q'*
1	0		
0	0		
0	1		
0	0		
1	1		

3. Observe the combination for which no change and invalid or race conditions arise.

Job 2:

Design of an SR Flip-flop using NAND gates only.



Procedure:

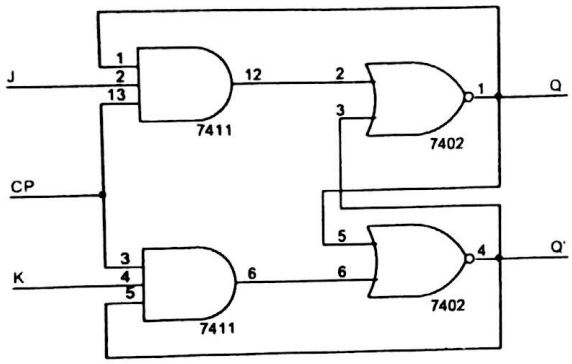
1. Draw the logic diagram to implement SR Flip-flop.
2. Fill up the table with different combination of inputs.

S	R	Q	Q'
1	0		
0	0		
0	1		
0	0		
1	1		

3. Observe the combination for which no change and invalid or race conditions arise.

Job 3:

Design of a J-K Flip-flop using AND & NOR gate only.



Procedure:

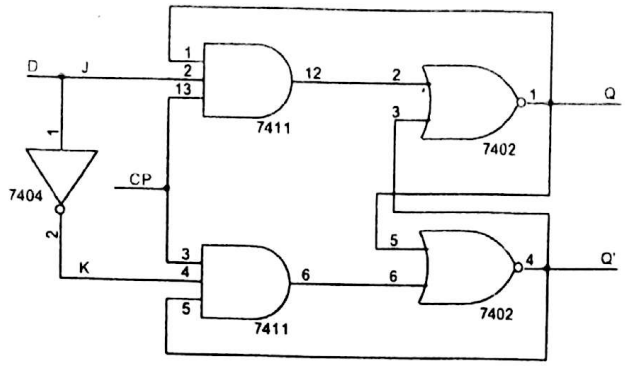
1. Draw the logic diagram to implement J-K Flip-flop.
2. Fill up the table with different combination of inputs.

Q	J	K	$Q(t+1)$
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

3. Observe the combination for which no change and invalid or race conditions arise.

Job 4:

Design of a D Flip-flop from a J-K Flip-flop.



Procedure:

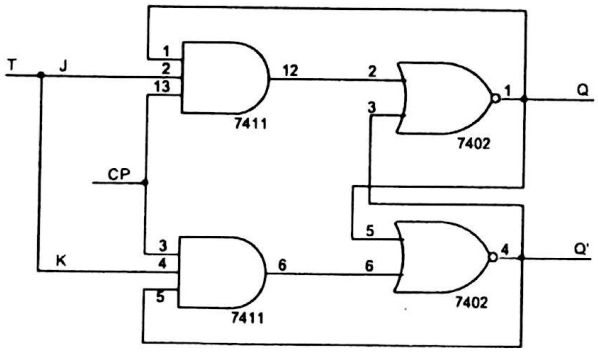
1. Draw the logic diagram to implement D Flip-flop.
2. Fill up the table with different combination of inputs.

Q	D	$Q(t+1)$
0	0	
0	1	
1	0	
1	1	

3. Observe the combination for which no change and invalid or race conditions arise.

Job 5:

Design of a T Flip-flop from a J-K Flip-flop.



Procedure:

1. Draw the logic diagram to implement T Flip-flop.
2. Fill up the table with different combination of inputs.

Q	T	$Q(t+1)$
0	0	
0	1	
1	0	
1	1	

3. Observe the output logic.